2015 IEEE VLSI PROJECT TITLES - R

S.No	VLSI
1	40-Gb/s 0.7-V 2:1 MUX and 1:2 DEMUX with Transformer- Coupled Technique for SerDes Interface
2	A 0.25-V 28-nW 58-dB Dynamic Range Asynchronous Delta Sigma Modulator in 130-nm Digital CMOS Process
3	A 2.5-Gb/s DLL-Based Burst-Mode Clock and Data Recovery Circuit With 4× Oversampling
4	A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes
5	A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT
6	A Dynamically Reconfigurable Multi-ASIP Architecture for Multistandard and Multimode Turbo Decoding
7	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications
8	A High-Throughput VLSI Architecture for Hard and Soft SC-FDMA MIMO Detectors
9	A Low Power and High Sensing Margin Non-Volatile Full Adder Using Racetrack Memory
10	A Low-Cost Hardware Architecture for Illumination Adjustment in Real-Time Applications
11	A Low-Cost Low-Power All-Digital Spread-Spectrum Clock Generator
12	A New Efficiency-Improvement Low-Ripple Charge-Pump Boost Converter Using Adaptive Slope Generator With Hysteresis Voltage Comparison Techniques
13	A New Parallel VLSI Architecture for Real-time Electrical Capacitance Tomography
14	A novel approach to realize Built-in-self-test(BIST) enabled UART using VHDL
15	A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders
16	A Novel Photosensitive Tunneling Transistor for Near-Infrared Sensing Applications: Design, Modeling, and Simulation
17	A Relative Imaging CMOS Image Sensor for High Dynamic Range and High Frame-Rate Machine Vision Imaging Applications
18	A Voltage Monitoring IC With HV Multiplexer and HV Transceiver for Battery Management Systems
19	Accelerating Scalar Conversion for Koblitz Curve Cryptoprocessors on Hardware Platforms
20	Aging-Aware Reliable Multiplier Design with Adaptive Hold Logic
21	Algorithm and Architecture Design of the H.265/HEVC Intra Encoder
22	All Digital Energy Sensing for Minimum Energy Tracking
23	An Analytical Framework for Evaluating the Error Characteristics of Approximate Adders
24	An Efficient Constant Multiplier Architecture Based on Vertical- Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis – *FIR FILTER*
25	An Efficient List Decoder Architecture for Polar Co
26	Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator
27	Architecture for Monitoring SET Propagation in 16-bit Sklansky Adder
28	Area-Efficient 3-Input Decimal Adders Using Simplified Carry and Sum Vectors
29	Comparative Performance Analysis of the Dielectrically Modulated Full-Gate and Short-Gate Tunnel FET-Based Biosensors
30	Design and Analysis of Inexact Floating-Point Adders
31	Design Flow for Flip-Flop Grouping in Data-Driven Clock Gating
32	Design of Efficient Content Addressable Memories in High- Performance FinFET Technology
33	Design of Self-Timed Reconfigurable Controllers for Parallel Synchronization via Wagging
34	Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA
35	Energy Consumption of VLSI Decoders

36	Exact and Approximate Algorithms for the Filter Design Optimization Problem
37	Fast Code Design for Overloaded Code-Division Multiplexing Systems
38	Fine-Grained Access Management in Reconfigurable Scan Networks
39	FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems
40	Fully Pipelined Low-Cost and High-Quality Color Demosaicking VLSI Design for Real-Time Video Applications
41	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications
42	Graph-Based Transistor Network Generation Method for Supergate Design
43	High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design
44	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels
45	High-Throughput LDPC-Decoder Architecture Using Efficient Comparison Techniques & Dynamic Multi-Frame Processing Schedule
46	Implementation of Subthreshold Adiabatic Logic for Ultralow- Power Application
47	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers
48	Integrating Lock-Free and Combining Techniques for a Practical and Scalable FIFO Queue
49	Learning Weighted Lower Linear Envelope Potentials in Binary Markov Random Fields
50	Level-Converting Retention Flip-Flop for Reducing Standby Power in ZigBee SoCs
51	Long-Distance Measurement Applying Two High-Stability and Synchronous Wavelengths
52	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication
53	MAC With Action-Dependent State Information at One Encoder
54	Minimum Parallel Binary Adders with NOR (NAND) Gates
55	Modified Wallace Tree Multiplier using Efficient Square Root Carry Select Adder
56	Modulation Classification of Single-Input Multiple-Output Signals Using Asynchronous Sensors
57	Novel Block-Formulation and Area-Delay-Efficient Reconfigurable Interpolation Filter Architecture for Multi-Standard SDR Applications
58	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System – *FIR FILER*
59	Novel Reconfigurable Hardware Architecture for Polynomial Matrix Multiplications
60	Obfuscating DSP Circuits via High-Level Transformations
61	One Minimum Only Trellis Decoder for Non-Binary Low-Density Parity-Check Codes
62	Partially Parallel Encoder Architecture for Long Polar Codes
63	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding
64	Range Unlimited Delay-Interleaving and –Recycling Clock Skew Compensation and Duty-Cycle Correction Circuit
65	Recursive Approach to the Design of a Parallel Self-Timed Adder
66	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations
67	Revisiting Central Limit Theorem: Accurate Gaussian Random Number Generation in VLSI
68	Shift Register Design Using Two Bit Flip-Flop
69	Signal Design for Multiple Antenna Systems With Spatial Multiplexing and Noncoherent Reception
70	Synthesis of Genetic Clock with Combinational Biologic Circuits
71	Timing Error Tolerance in Small Core Designs for SoC Applications
72	Two-Step Optimization Approach for the Design of Multiplierless Linear-Phase FIR Filters
73	VLSI-Assisted Non-rigid Registration Using Modified Demons Algorithm

PROJECT SUPPORT TO REGISTERED STUDENTS:

1) IEEE Base paper.
2) Abstract Document.
3) Future Enhancement (based on Requirement).
4) Modified Title / Modified Abstract (based on Requirement).
5) Complete Source Code.
6) Final Report / Document
· 100% Assurance for Project Execution

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